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Challenges of EUV lithography for HVM

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  - 1st step for HVM; requirements for pilot production
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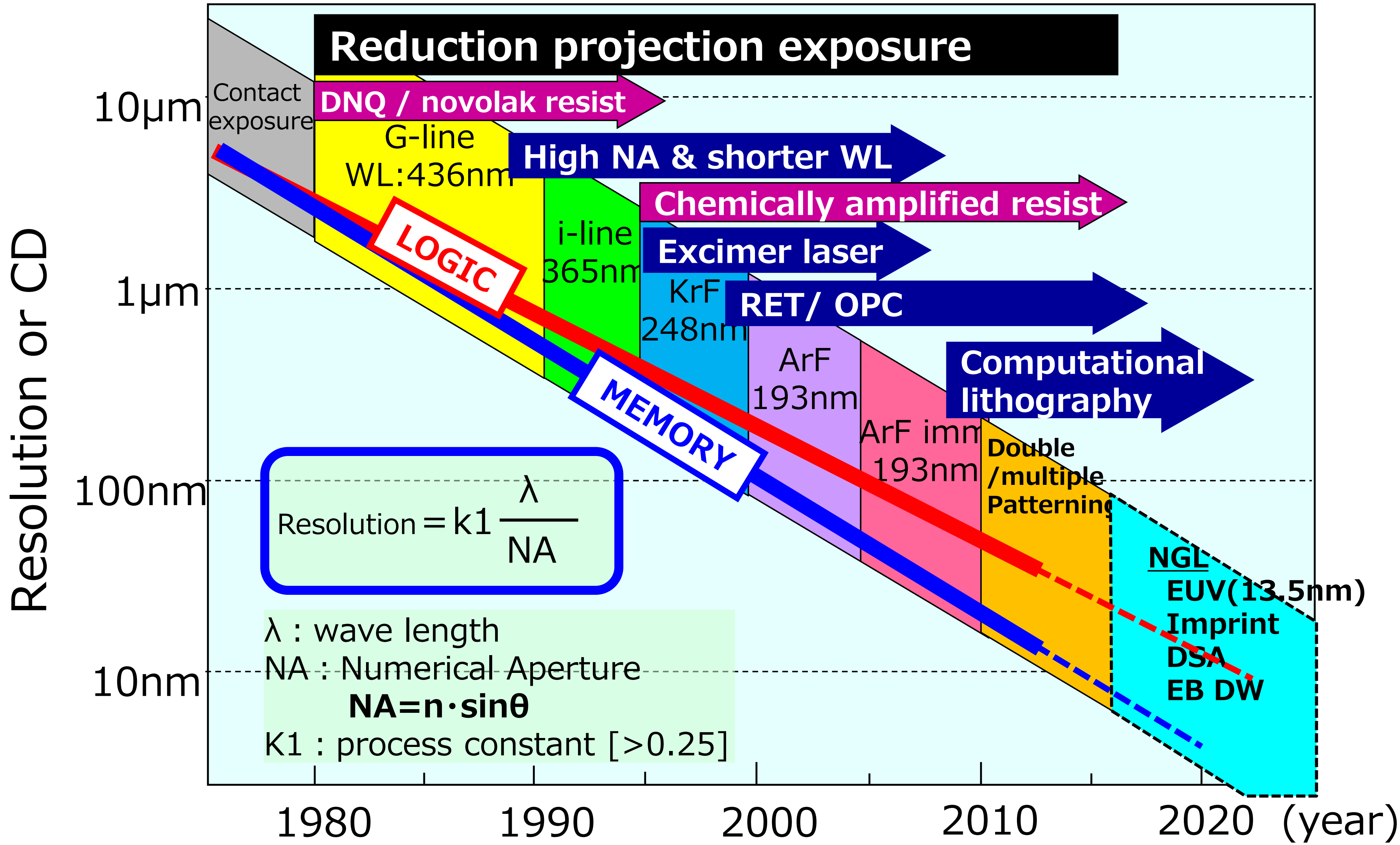
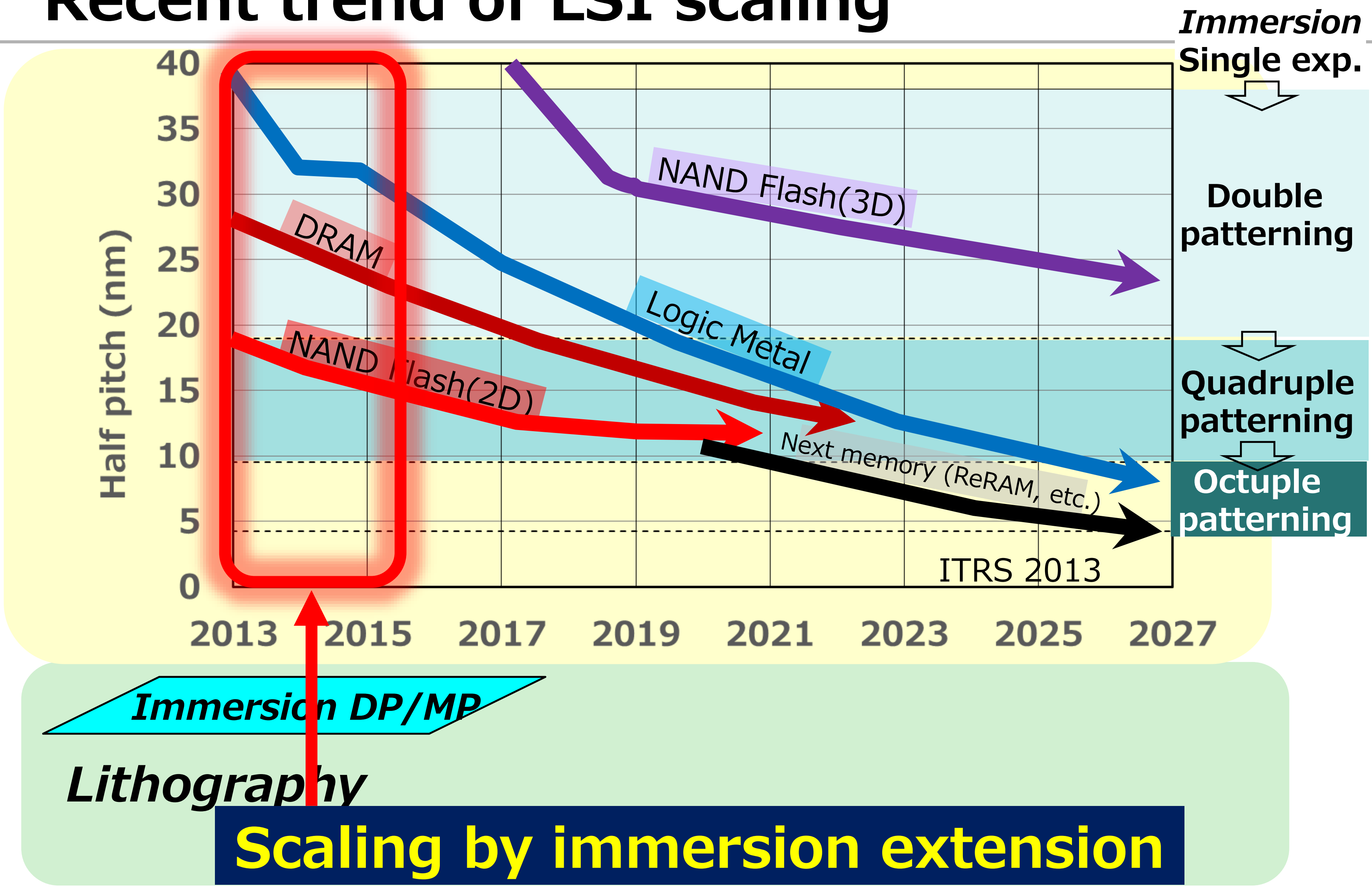
Introduction

Lithography Challenges

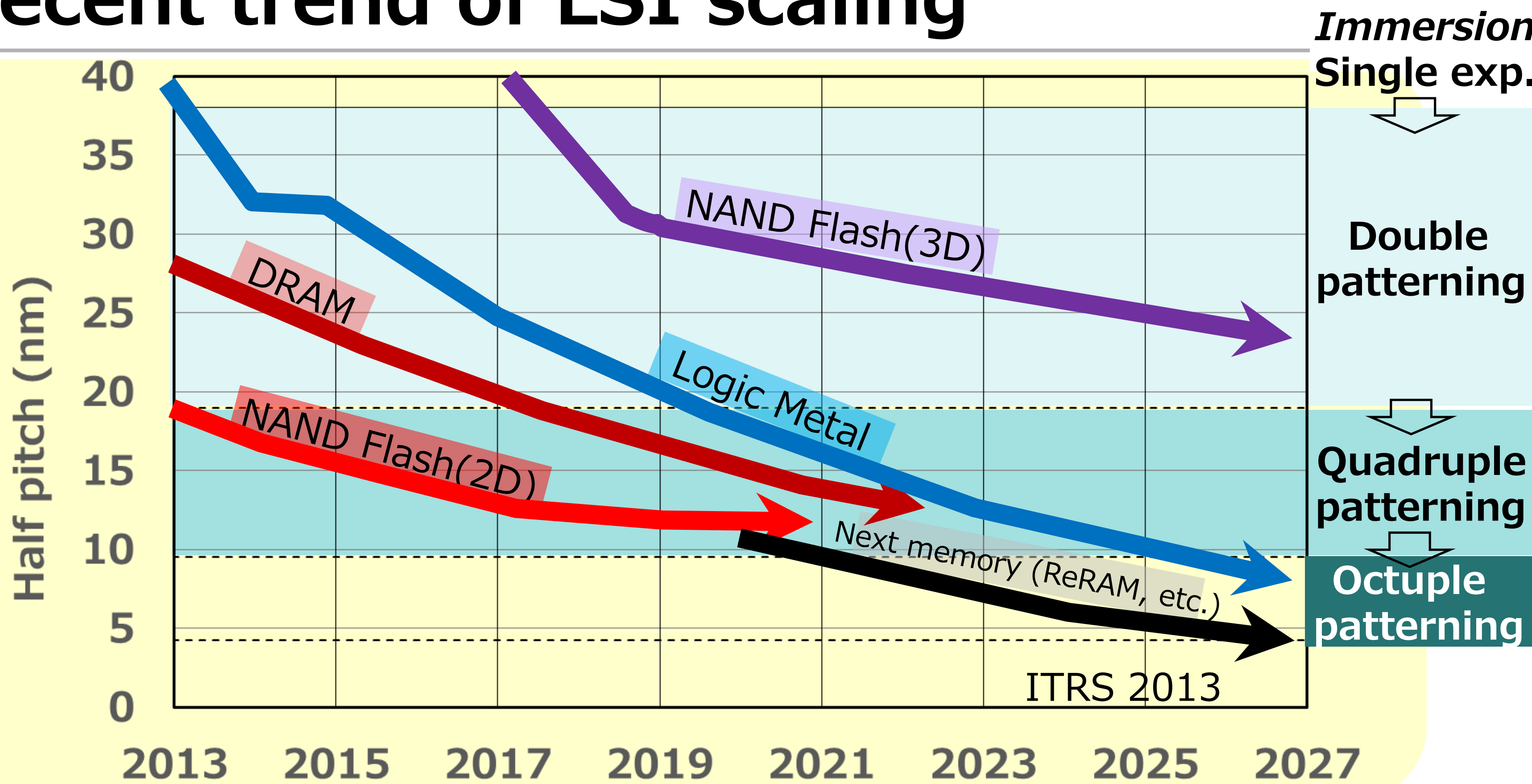
Lithography history

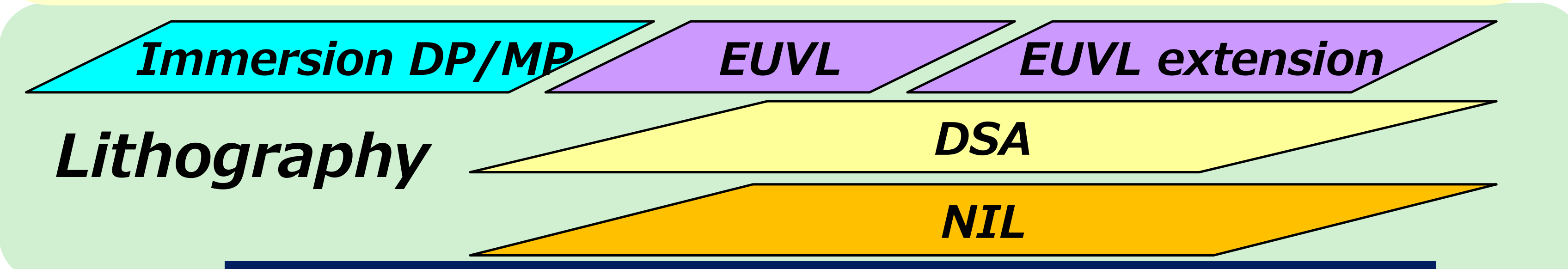


Recent trend of LSI scaling



Recent trend of LSI scaling





Cost effective is 1st priority

EUVL has potential of high resolution.

$$\text{Resolution} = k1 \frac{\lambda}{NA}$$

λ : exposure wavelength
NA : Numerical Aperture
k1 : process constant[>0.25]

NA \ k1	0.40	0.35	0.30	0.25
0.25	21.6	18.9	16.2	13.5
0.30	18.0	15.8	13.5	11.3
0.33	16.4	**14.3**	12.3	10.2
0.35	15.4	13.5	11.6	9.6
0.40	13.5	11.8	10.1	8.4
0.45	12.0	10.5	9.0	7.5
0.50	10.8	9.5	8.1	6.8
0.55	9.8	8.6	7.4	6.1
0.60	9.0	7.9	6.8	5.6
0.65	8.3	7.3	6.2	5.2
0.70	7.7	6.8	5.8	4.8

Resolution → less than 10 nm

History of lithography potential solutions of ITRS

	ArF	F2	ArF i	ArF HI	DP	MP	PXL	EUV	IPL	EPL	NIL	ML2	DSA	6.Xnm
1992	250						250	180	180	180		130		
1994	180						250	100	130	130		130		
1997	130						130	130	130	130		130		
1999	130	100					100	70	100	100		70		
2001	110	90					65	65	65	90		65		
2003	110	65	65				X	45	X	65	32	45		
2005	90	X	65	45				45		X	32	45		
2007			65	32	45			32			32	32	22	
2009														
2011					22	22		22			22	22	16	11
2013					30-20	19-16		19-16			14-11	14-11	19-16	

HVM

So, we wait for EUVL long time.

National project for EUVL in Japan

1985

1986: Experimental trial of EUV projection exposure by H. Kinoshita of NTT, et al.

1990

1992~95: SORTEC
(mask, illumination and proc development by Nikon and Hitachi)

1995

1998~2006: ASET (process, k and metrology)

2000

2001~10: MIRAI (mask n logy)

2002~11: EUVA
(source, exposure tool a optics metrology)

2005

2006 **ASML**
Full field scanner; ADT

2003~07: Leadin (source)

2010

2010~ **ASML**
Pre production tool; 3100

2006~11: Selete
(full field scanner, m metrology)

2013~ **ASML**
Production tool; 3300

2015

2012~: EIDEC (mask metr nd resist)

202

High NA scanner

30 years anniversary in 2016➔ HVM will start !?

Challenges of EUV lithography for HVM

Focus area of EUV lithography

2011 / 22hp	2012 / 22hp	2013 / 22hp	2014 / 16hp
1. Long-term reliable source operation with 200 W at IF	1.Long-term reliable source operation with a. 200 W at IF in 2014 b. 500 W-1,000 W in 2016	1.Long-term reliable source operation with a. 125 W at IF in 2014 b. 250 W in 2015	1. Reliable source operation with > 75% availability – 125 W at IF in 1H / 2015 (at customer)) – 250 W at IF in 1H / 2016 (HVM entry at customer)
2. Mask yield & defect inspection/review infrastructure	2. Mask yield & defect inspection/review infrastructure	2. Defect free masks through lifecycle & inspection/review infrastructure	2. Resist resolution, sensitivity & LER met simultaneously – Progress insufficient to meet 2015 introduction target
3. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously	3. Keeping mask defect free - Availability of pellicle mtg HVM req't - Minimize defect adders during use	3. Mask yield & defect inspection/review infrastructure – Enable high yield defect free mask blank supply chain
• EUVL manufacturing integration	• EUVL manufacturing integration	4. Resist resolution, sensitivity & LER met simultaneously	4. Keeping mask defect free – Availability of pellicle mtg HVM req't : need integrated industry strategy for solution –Minimize defect adders during use

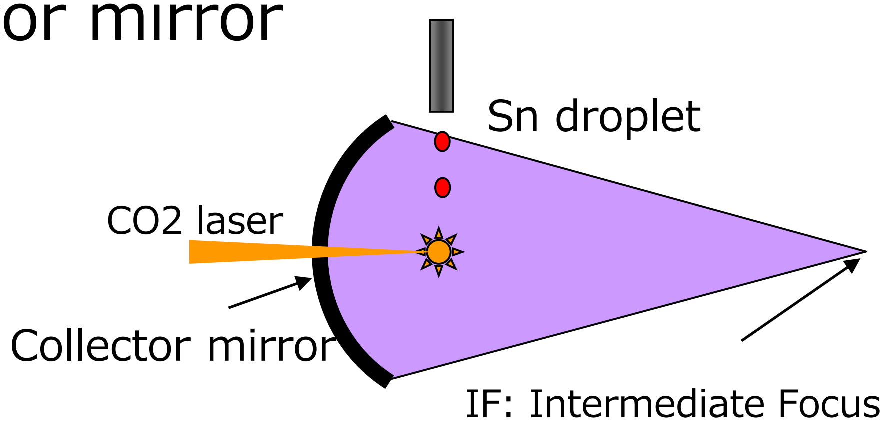
Ranked by 13th International EUVL Symposium Program Steering Committee, Washington, D.C. October 29, 2014

1st step for HVM

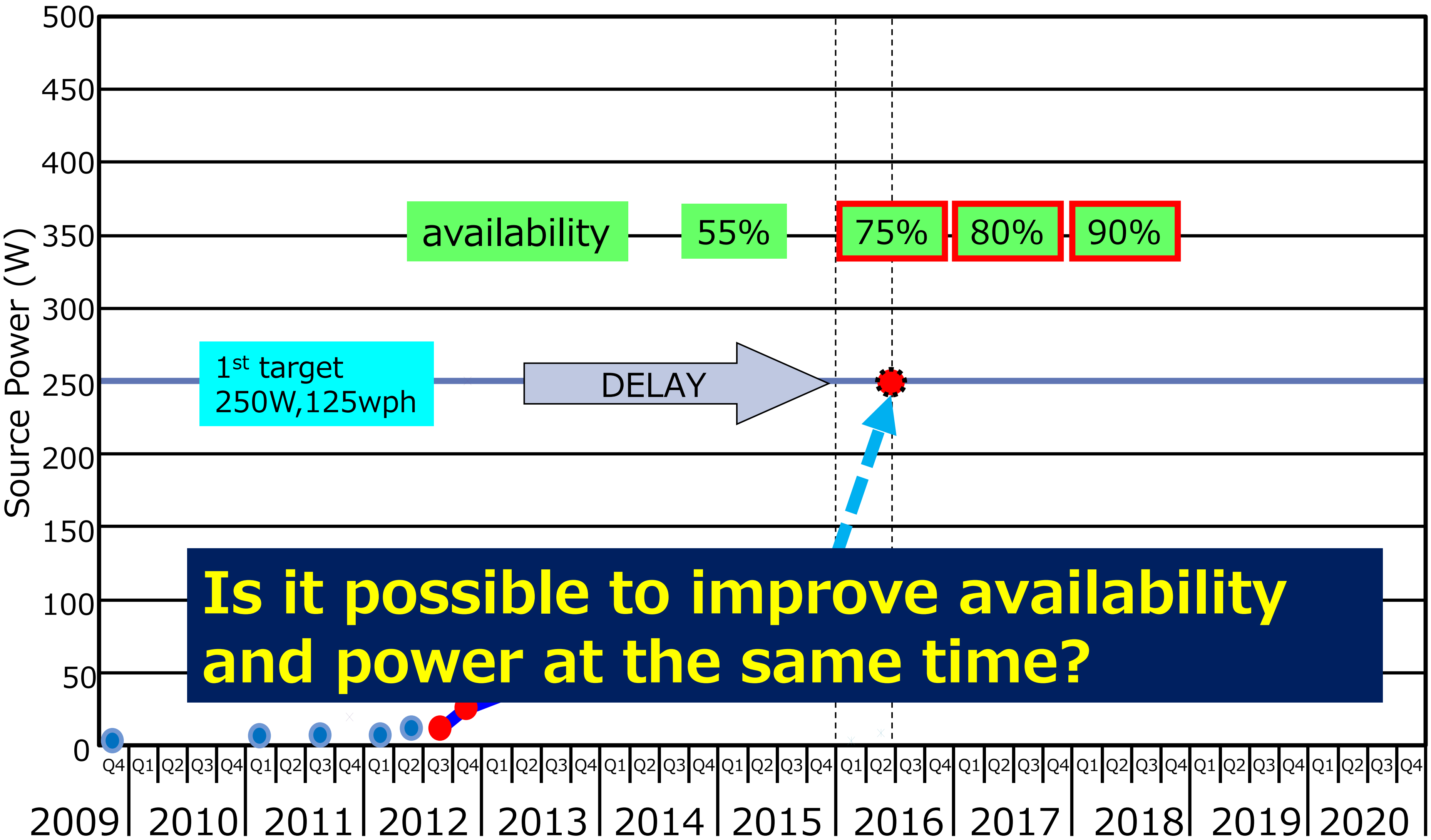
- **Requirements for pilot production**
  - Acceptable performance for pilot production
    - Throughput with source power of > **100 W**
    - Tool availability more than **75 %**
    - Lithographic performance (CDU, LWR, OL)
    - Process **repeatability**
    - Defectivity to keep available yield for device evaluation
      - Defectivity of mask blank and mask pattern
      - Pellicle ~ T = 85 %
      - Resist process defectivity

Source power for pilot production

- **LPP(Laser Produced Plasma) source**
  - **Current power ~100 W, availability ~ 55 %**
  - Challenges
    - More availability
    - Operational cost reduction
      - Debris mitigation
      - Droplet generator
      - Collector mirror



EUV source power



RLS trade off of EUV resist

- **<u>R</u>esolution: target ≤ 16 nm LS**
  - Resolution of EUV resist is not enough, higher k1 (poorer) than ArF.
    - 14nm LS(NA=0.33)~k1=<u>0.34</u>(CAR)~ worse LWR
    - 13nm LS(NA=0.33)~ ~k1=<u>0.32</u>(non-CAR)~ lower sensitivity
  - LS pattern of ArF resist~ k1=<u>0.26</u>, 2D pattern~ k1=<u>0.31</u>

NA \ k1	0.44 **EUV resist** (2D)	0.34 **EUV resist** (LS)	0.31 **ArF resist** (2D)	0.26 **ArF resist** (LS)
0.25	23.8	18.4	16.7	14.0
0.30	19.8	15.3	14.0	11.7
0.33	18	**<u>13.9</u>**	12.7	10.6
0.35	17	13.1	12.0	10.0
0.40	14.9	11.5	10.5	**8.8**
0.45	13.2	10.2	**9.3**	**7.8**
0.50	11.9	**9.2**	**8.4**	**7.0**
0.55	10.8	**8.3**	**7.6**	**6.4**
0.60	9.9	**7.7**	**7.0**	**5.9**
0.65	9.1	**7.1**	**6.4**	**5.4**
0.70	8.5	**6.6**	**6.0**	**5.0**

2D pattern by EUVL

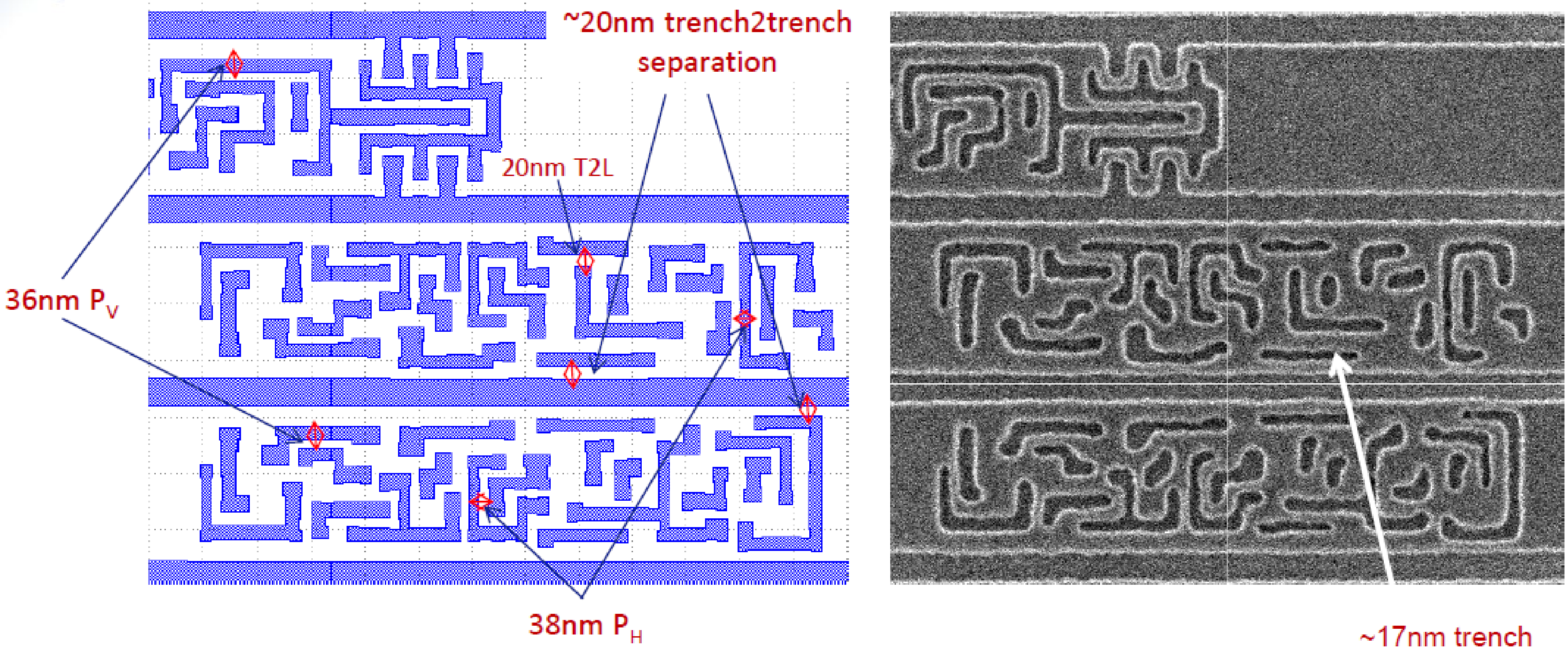
Courtesy of ASML

N7 Logic : Routed 2D semi-gridded Metal 1

36x38nm (PV x PH)

ASML

Public
Slide 1
15 April 2015



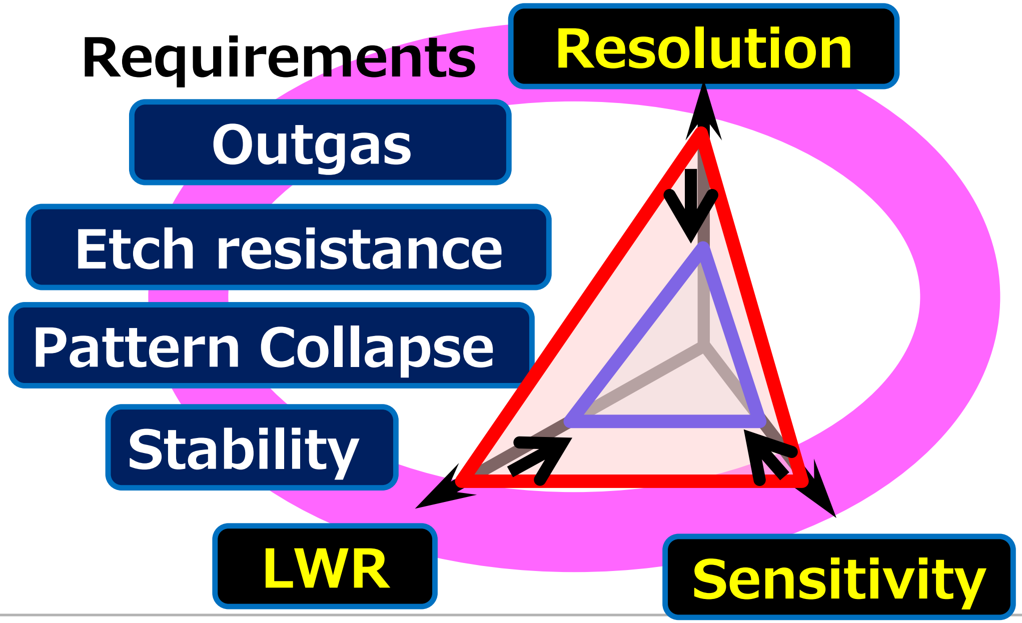
This example would require 4 exposures with 193 immersion – or one with 0.33NA EUVL

Conditions: NXE:3300B, annular illumination, 60nm resist, 40mJ/cm2 dose

RLS trade off of EUV resist

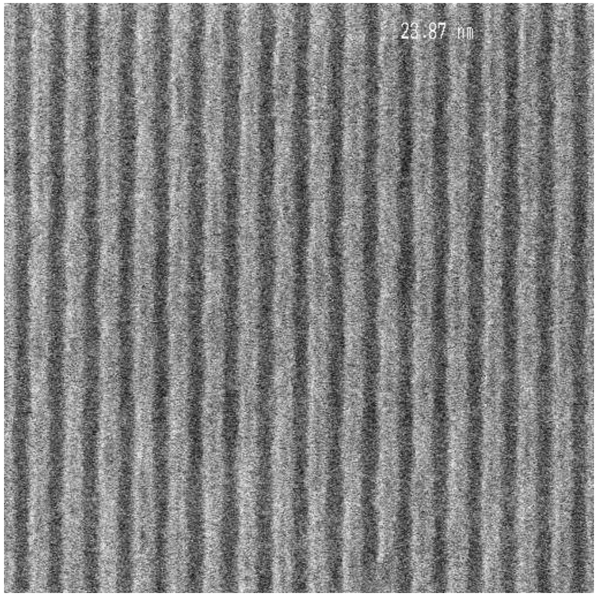
- **LWR: target ≤ 3 nm**
  - Current level is >5 nm@ 16nm LS
  - Additional process can improve LWR of high frequency.
  - **It is very difficult to improve LWR of low frequency.**
  - **Etch resistance should be improved.**

- **Sensitivity: target ≤20mJ/cm²**
  - CAR: ~ 40 mJ/cm²

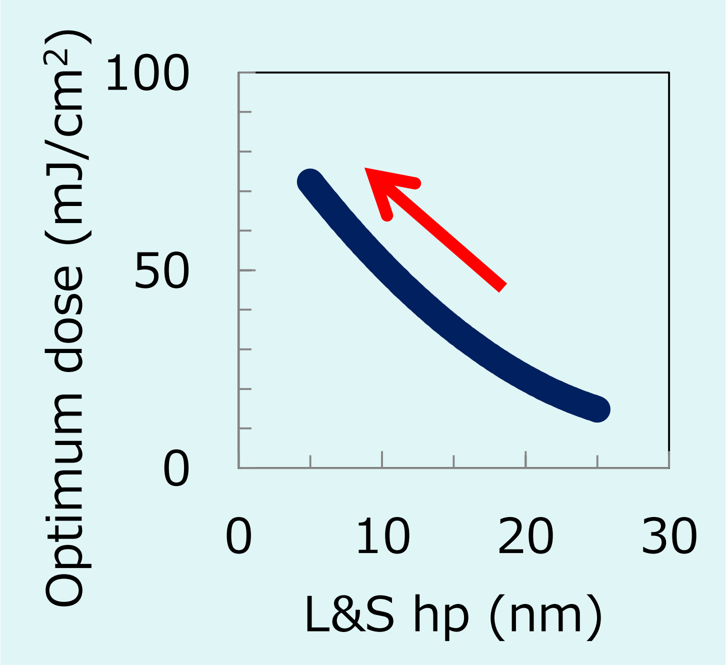


EVU resist

- **It becomes harder to achieve RLS trade off for smaller CD.**
  - **CAR: LER / LWR**
  - **Non-CAR: Sensitivity (>>60mJ/cm^2)**
  - **Etch resistance**



Example of resist pattern



Pattern size and dose

➔ Breakthrough of resist material
Paradigm shift to new platform

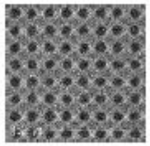
CDU

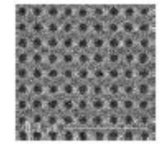
Courtesy of ASML

Imaging evaluation for ≤15nm DRAM storage node layer

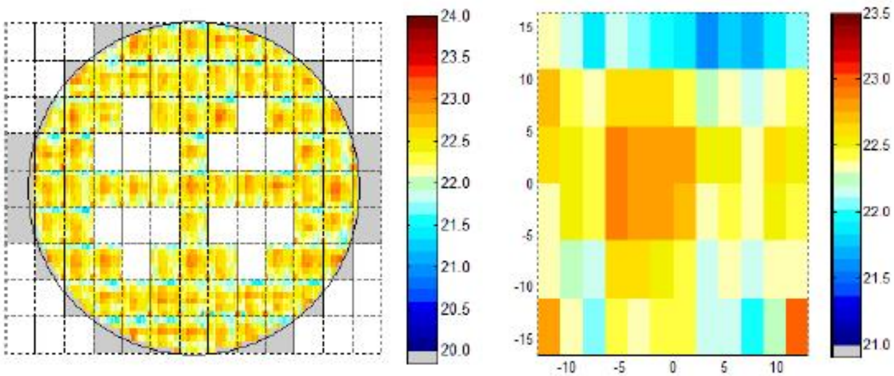
Preliminary results on a NXE:3300B

ASML
Public
Slide 2
15 April 2015





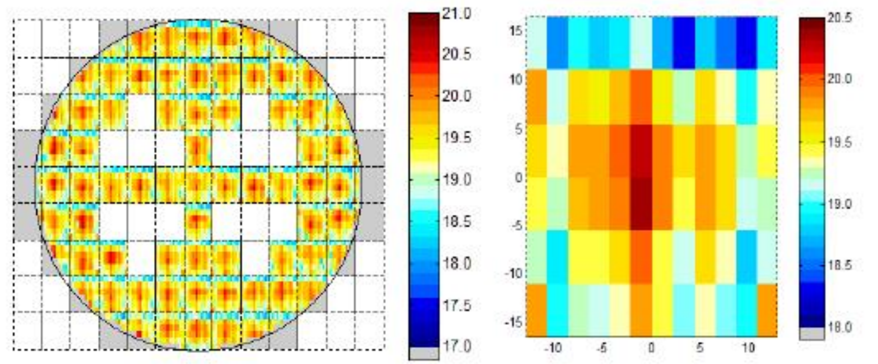
Dense CH – 20nm HP



CDU	CD	FW CDU
CH	22.4	1.0

Dose ≈ 37mJ/cm²

Dense CH – 18nm HP



CDU	CD	FW CDU
CH	19.4	1.4

Dose ≈ 49mJ/cm²

Experimental conditions

- *NA=0.33, sigma inner/outer=0.6/0.9 Quasar - 30*

CDU <1.5nm at ~ 80 W

EUV Mask Infrastructure Readiness

	hp2xnm	hp1xnm	
Multilayer Blank Inspection	DUV	Actinic	
Pattern Inspection	DUV	EB	Actinic
Particle Inspection	DUV/EB	EB	
Defect Repair	EB Repair	EB Repair	
Mask Defect QA	SEM + Litho. Simulation	SEM + Litho. Simulation	AIMS-EUV

ready

under developing

EUV pellicle

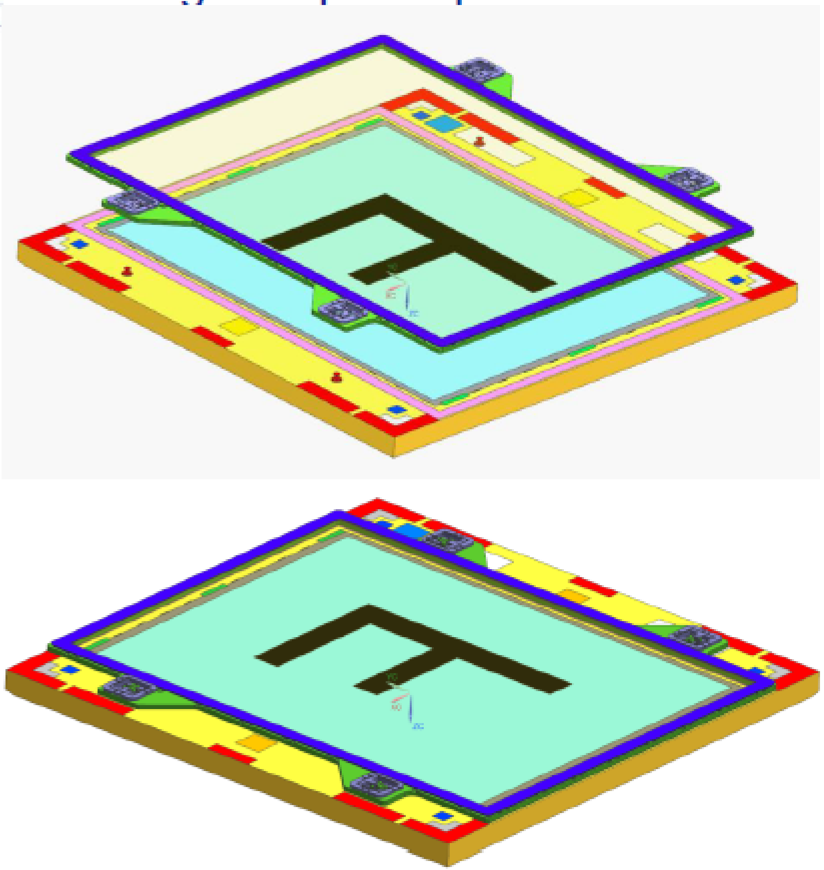
Courtesy of ASML

NXE Pellicle concept: particle free mounting/ de-mounting

ASML

Public
Slide 4
15 April 2015

Allowing multiple inspection schemes



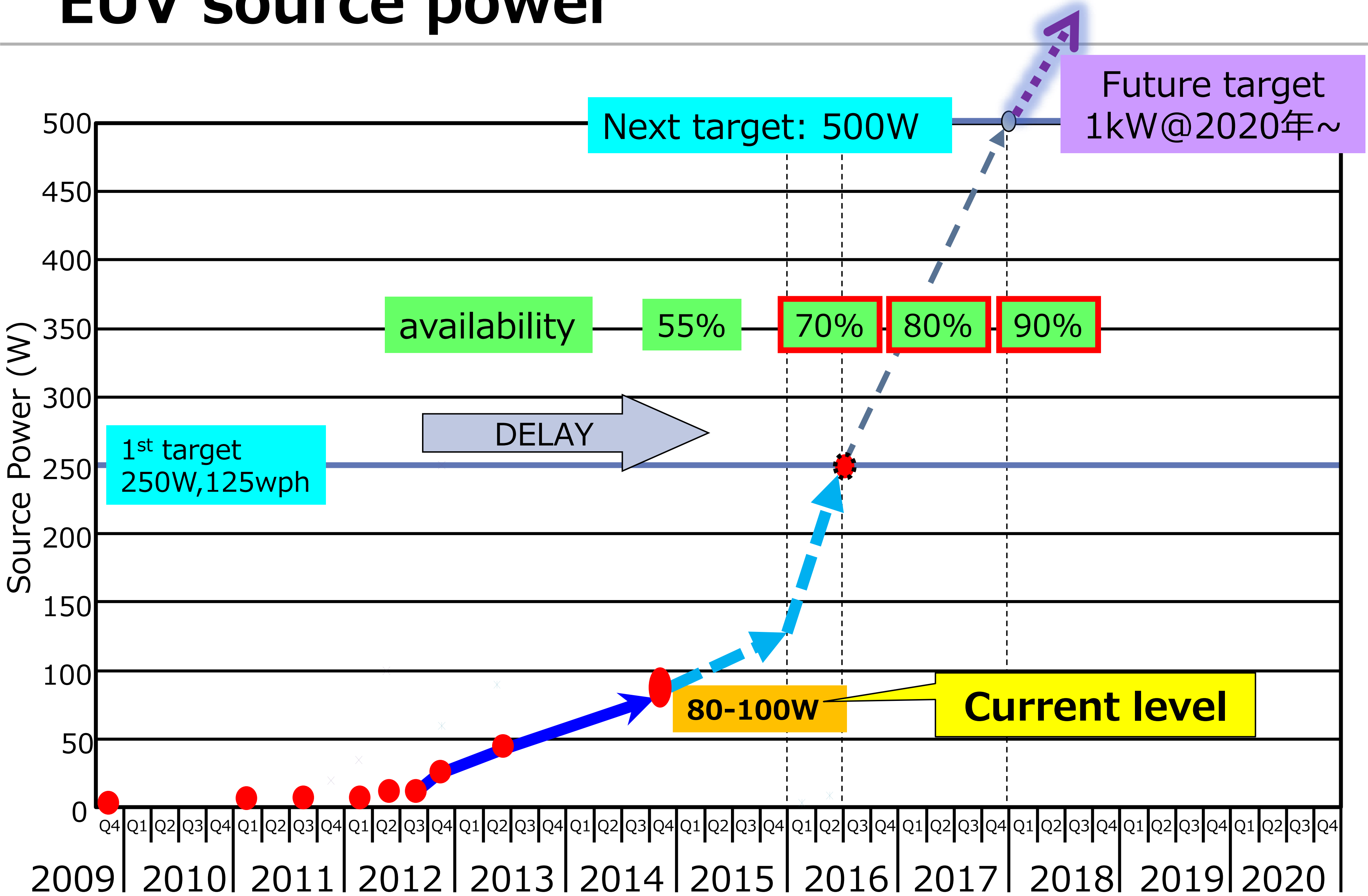
Key features

- Reticle front side defect-free solution
  - protects reticle front side from fall-on defects
  - particle free material combination and mounting technology to prevent particle generation
  - additional particle suppression towards pattern area
- Designed for use in NXE scanner
  - pump down/vent cycles compatible
  - vacuum and H_2 environment compatible
  - meets outgassing requirements
  - no overlay impact, distortion-free mounting
- Compatible with standard EUV mask flow
  - concept supports any type of pattern mask inspection: optical, e-beam, and actinic; both at mask shop and fab
  - allows for reticle repel cycle

2nd step for HVM

- **Requirements for high volume production**
  - Acceptable performance
    - **Ultimate high throughput** with > **250 W** source
    - Tool availability more than **95 %**
    - Lithographic performance (CDU, LWR, OL) with 250 W source i.e. **higher scanning speed**
    - Process **repeatability and stability** with **250 W source**, i.e. **higher temperature control**
    - Defectivity to keep **high yield for the real production**
      - The requirement level depends on type of device and design
      - Pellicle: **T > 90 % (= 20% loss of light intensity)**
  - Need maximum continuous efforts for the **lowest CoO**
    - Cost down of consumable parts and materials

EUV source power



Pattern shrink trend based on ITRS 2013

(Table ORTC & Table PIDS7b of ITRS 2013)

	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
Logic node	16/ 14		10		7		5		3.5		2.5		1.8		1.3
Logic Metal hp	40	32	32	28	25	23	20	18	16	14.2	12.6	11.3	10.0	8.9	8.0
Logic Fin hp	30	24	24	21	19	17	15	13	12	10.6	9.5	8.4	7.5	6.7	6.0
NAND Flash 2D	18	17	15	14	13	12	12								
NAND Flash 3D	64	54	54	45	45	32	30	29	28	27	27	26	25	24	23
DRAM	28	26	24	22	20	18	17	15	14	13	12	11	10	9.2	7.7
ReRAM						12	12	12	8	8	8	6	6	6	4

EUV(NA=0.33) Single

EUV(NA=0.33) DPT

EUV(NA=0.33) MPT

Single exposure by high NA EUV

EUV resist for high NA EUV

- **RLS trade off**
  - Difficult to overcome RLS trade off for smaller CD
  - More influence of shot noise in smaller CD. More dose will be required for smaller CD.
  - Resolution will become 1st priority, so sensitivity will be the last priority.
- **Etch resistance**
  - Resist thickness is reducing with scaling. Etch resistance should be kept at same level as ArF resist.
- **New platform materials**
  - Nano-particle resist
  - Inorganic resist
  - **Need new idea for break throough !!**

EUV scanner and source for high NA EUV

- **High power source of 500 ~ 1000 W**
  - Durability and heat treatment of all mirrors, mask and pellicle
  - Very high availability by short maintenance and longer lifetime of consumable parts
  - **XFEL is a candidate of the future source.**

- **Scanner**
  - Because high NA scanner will be very expensive, **higher throughput** and **ultimate availability** will be required strongly.
  - Smaller field size with 8X mask will lead high speed scanning stage in order to minimize the decrease of throughput.
  - Keeping 4X mask is the best way to achieve the highest TPT.

High power source

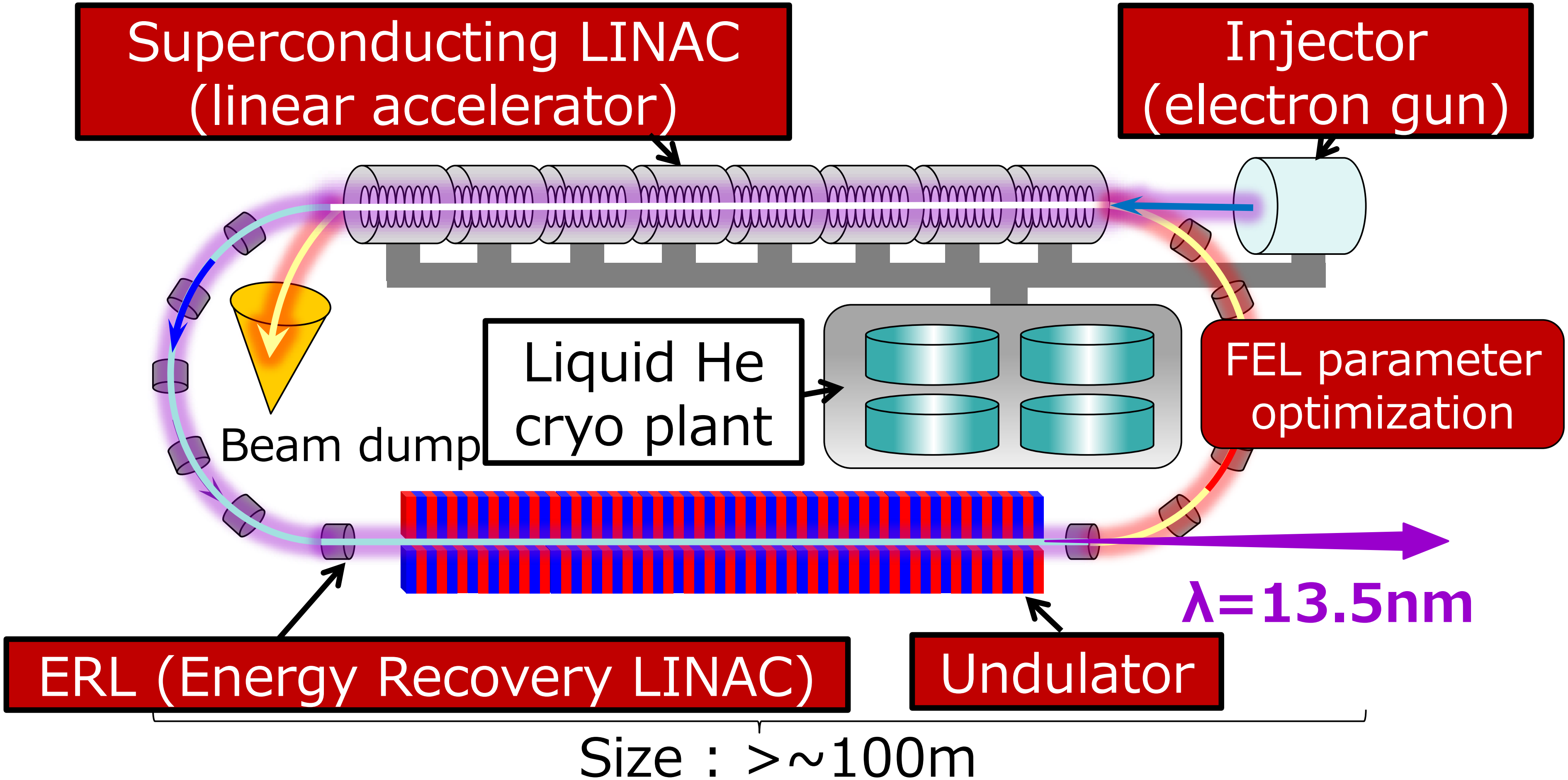
- **LPP(Laser Produced Plasma)**
  - **Current target: 250 W**
  - Scalability of LPP source to >> 250 W ??

- **EUV-FEL(Free Electron Laser)**
  - No experience in semiconductor industry
  - Still in the conceptual stage for λ = 13.5 nm

Concerns for EUV-FEL

- Proof of concept; λ=13.5 nm / > 10 kW
  - difficult to make a pilot system ~ takes long time to build
- Availability for 365D/24H
  - Redundancy system
- Impact for wafer cost
  - FEL cost is expected to be lower than LPP.
- Electrical power consumption
  - FEL will be better than LPP.
- Facility size
  - Very large underground facilities (> ~ 100 m)
- Timely readiness; long lead time items
  - Long term project management
- Coherence cause speckle noise and peak power cause damage
  - Need new idea for all reflective optics

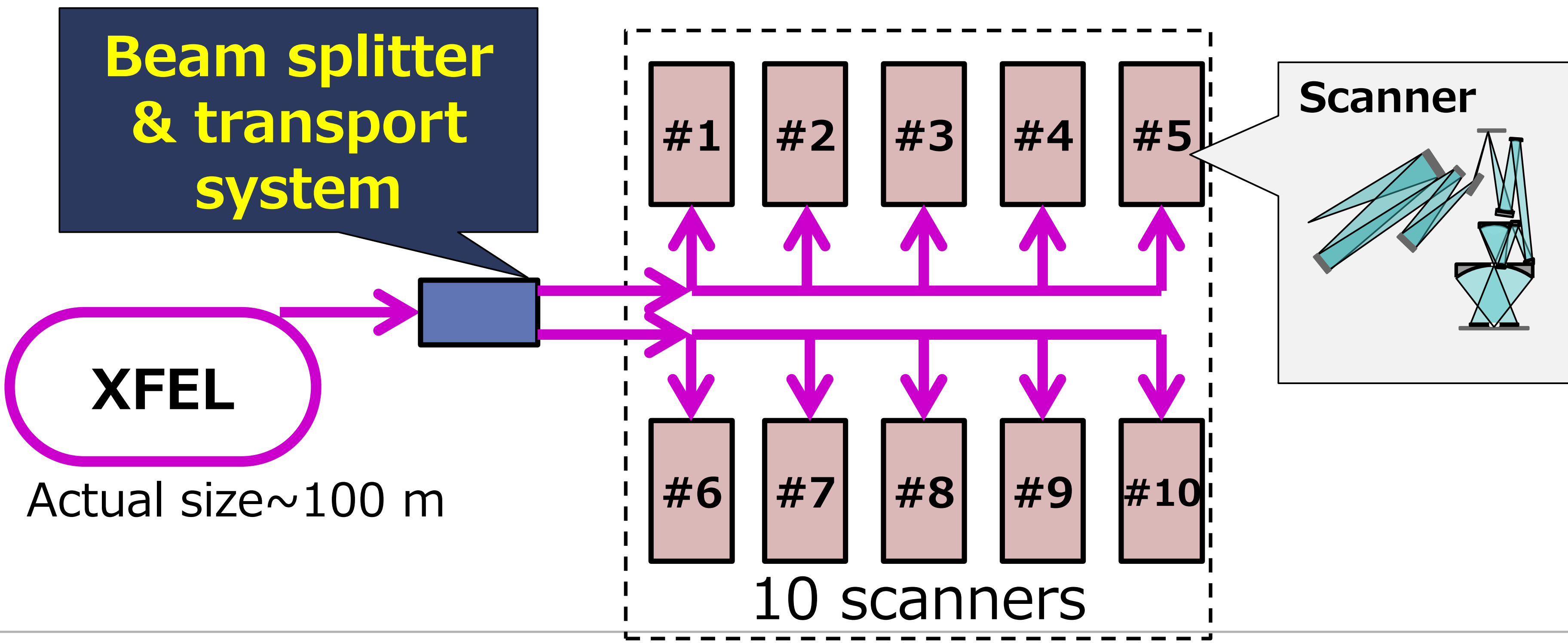
Key technologies of EUV-FEL



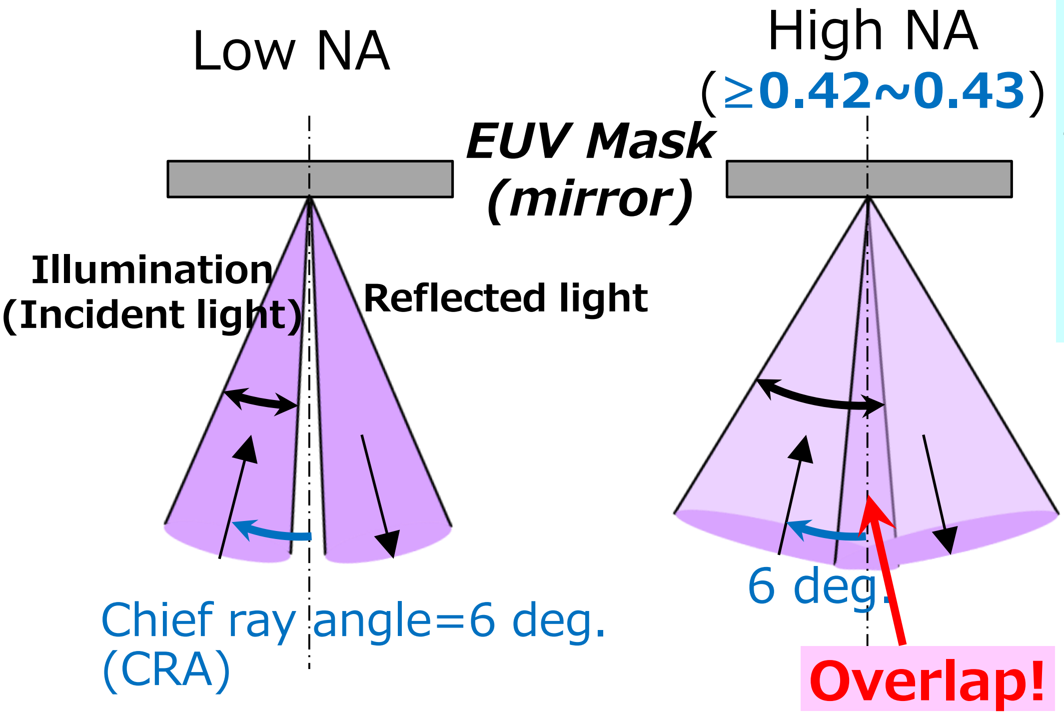
There are many challenges for high power EUV-FEL.
But nothing will be a show stopper, technically.
Careful and sufficient optimization will be required.

Optics for high NA and high power

- Speckle noise due to **high coherence**
- Damage due to **high power EUV light** for all optics (e. g. beam splitter and transport system, ML mirror, mask and pellicle)



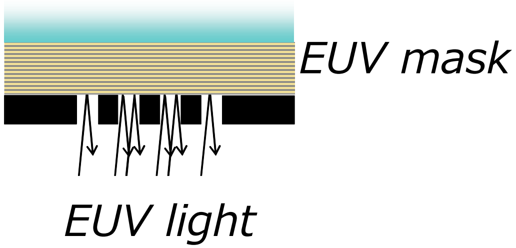
High NA EUV trade-off : EUV optics



Countermeasure

<u>1) Increasing CRA :</u> <u>Difficult</u>

Because of pattern shift in defocus due to mask 3D effect



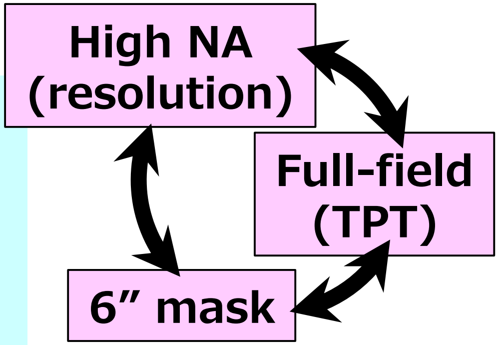
<u>2) Reduction ratio change from 1/4 to 1/6 ~ 1/8 with keeping CRA=6 deg.</u>

2-1) Increasing mask size to 9 inch . : Difficult

Because of the renewal of mask infrastructure

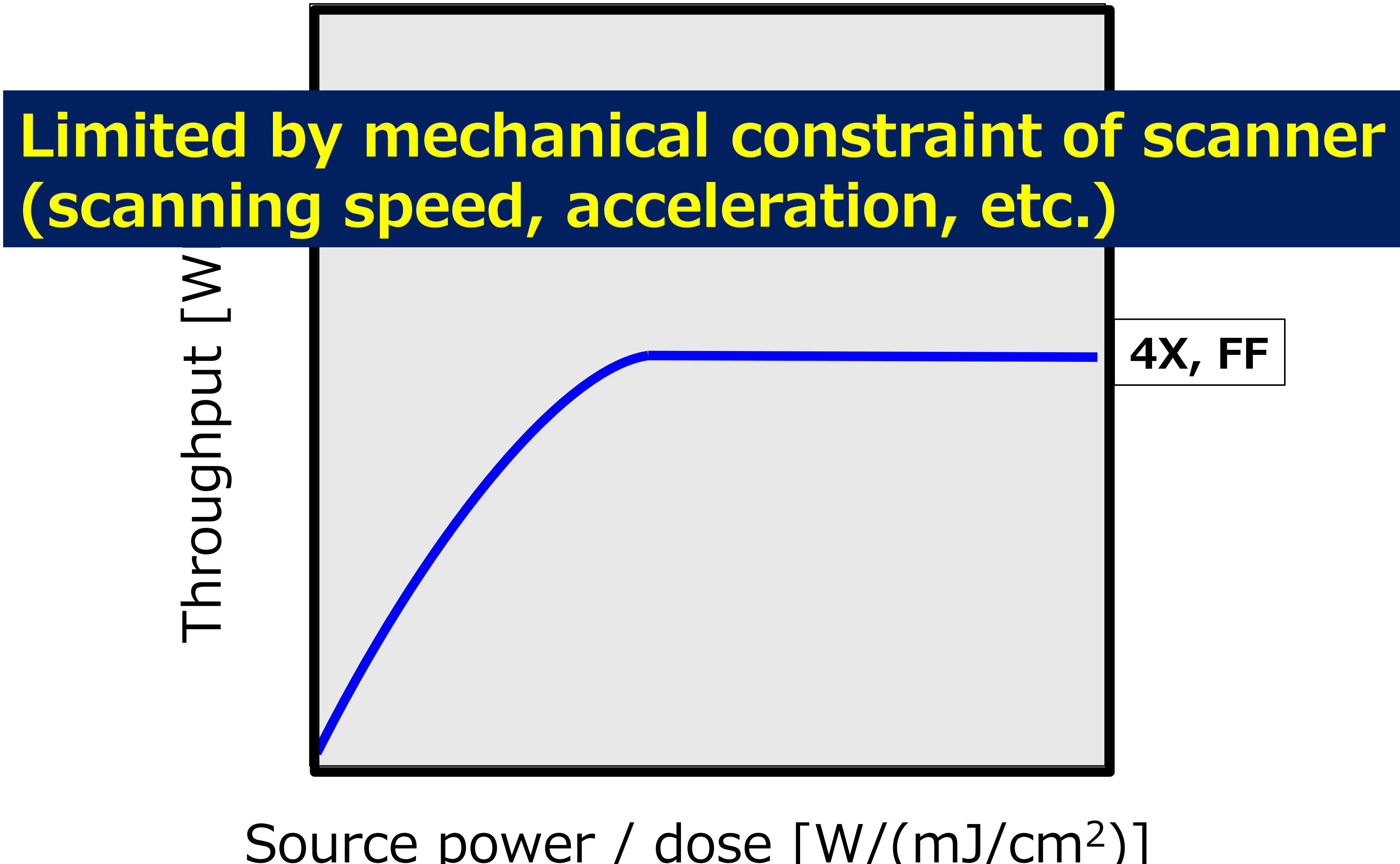
2-2) Decreasing of exposure field size to ½ or ¼

Challenge for TPT (concern about CoO)



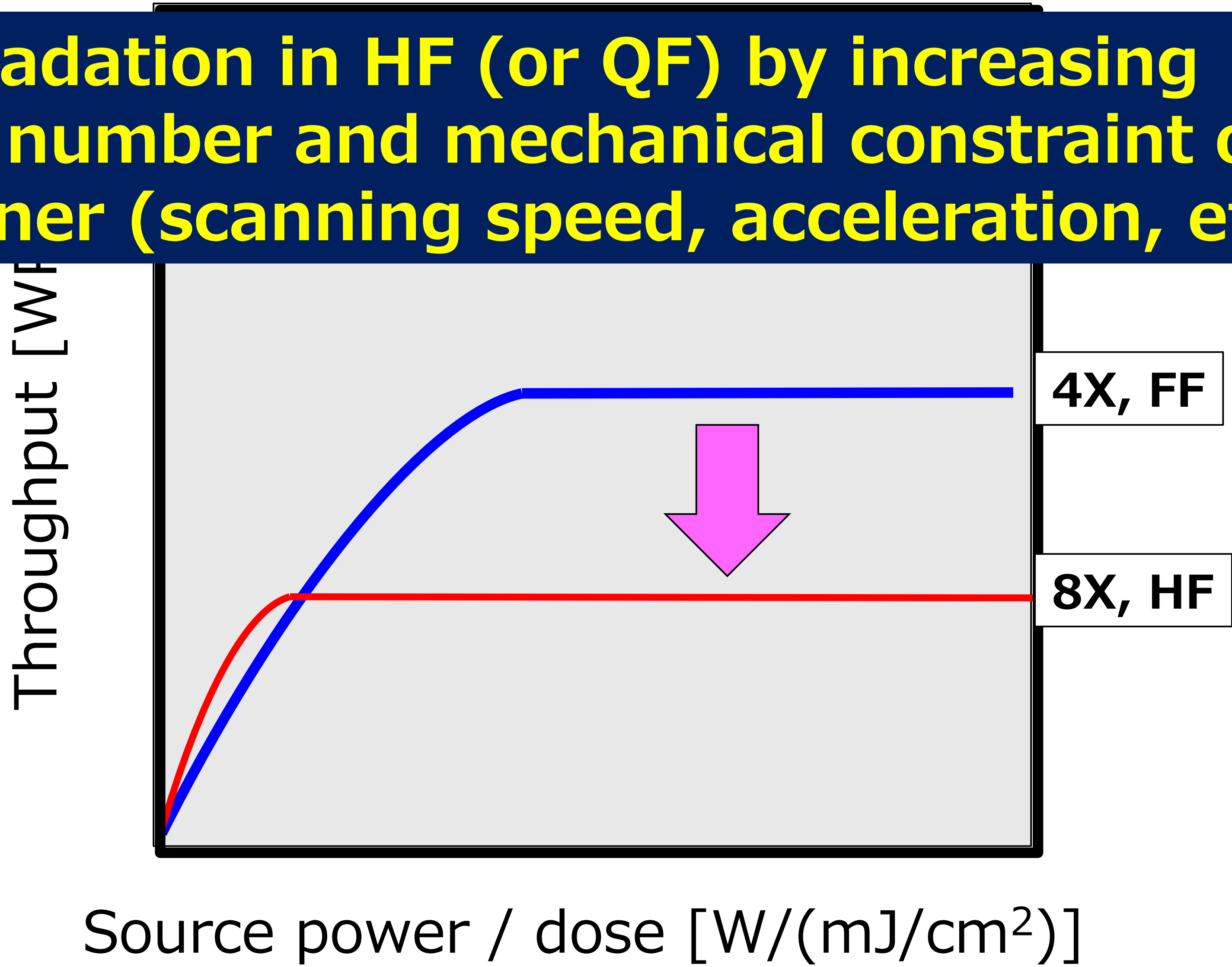
<u>ASML proposal: "HF"</u>
8X in scan direction
4X in other direction

Maximizing throughput of high NA EUV



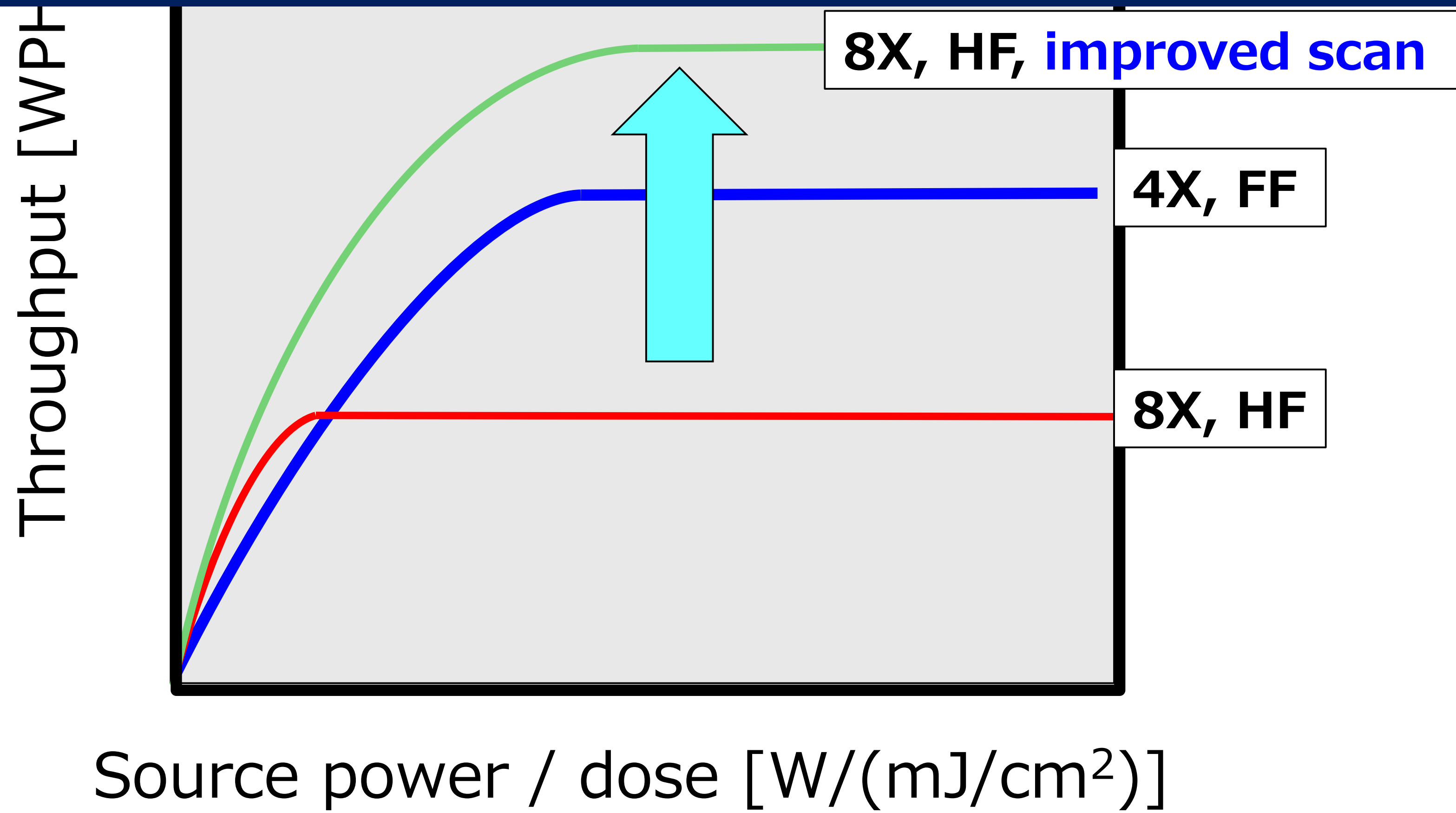
Maximizing throughput of high NA EUV

Degradation in HF (or QF) by increasing field number and mechanical constraint of scanner (scanning speed, acceleration, etc.)

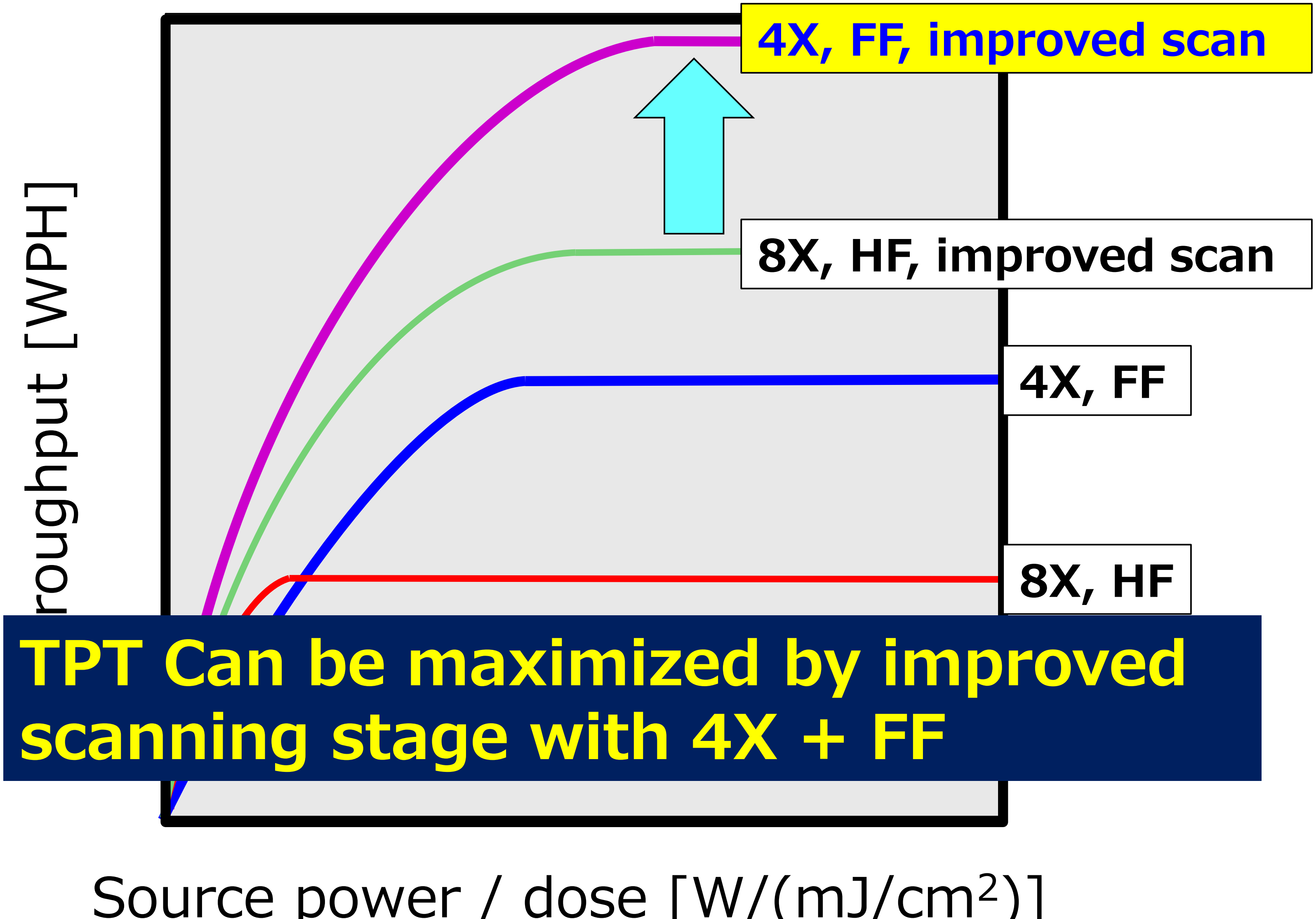


Maximizing throughput of high NA EUV

Improved scanning stage (higher scanning speed and higher acceleration, etc.)
But, not best solution !

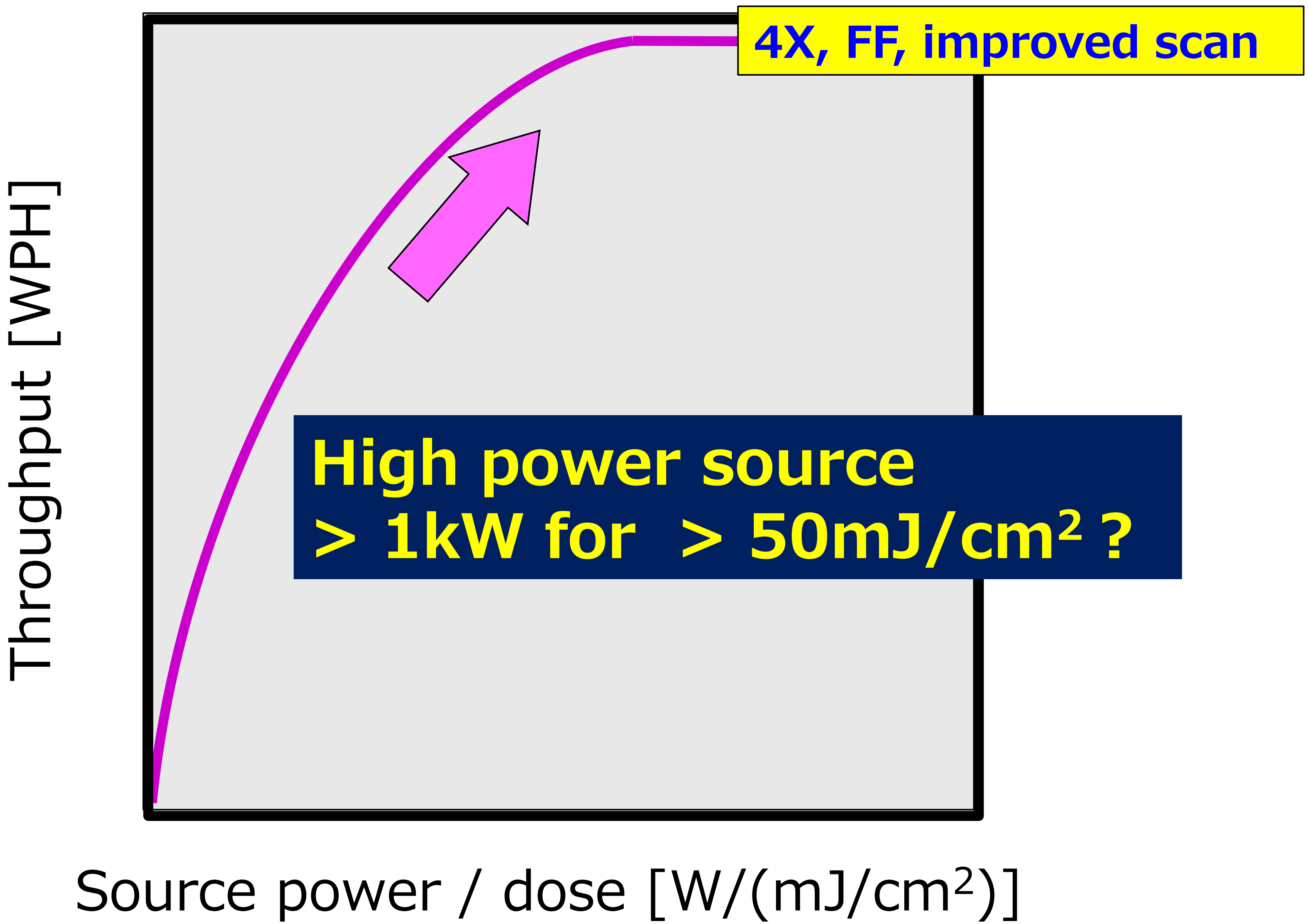


Maximizing throughput of high NA EUV



TPT Can be maximized by improved scanning stage with 4X + FF

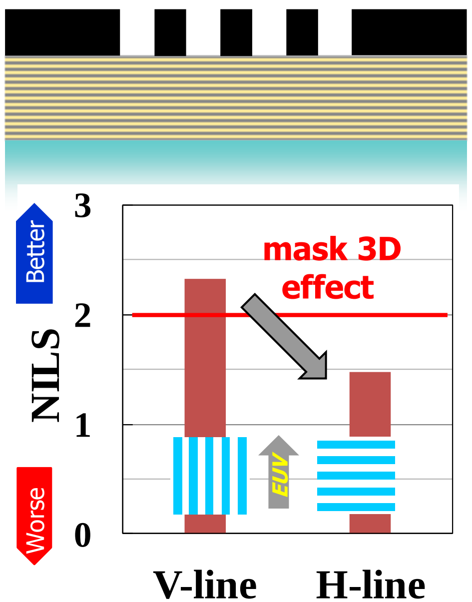
Maximizing throughput of high NA EUV



How to realize 4X mask for high NA

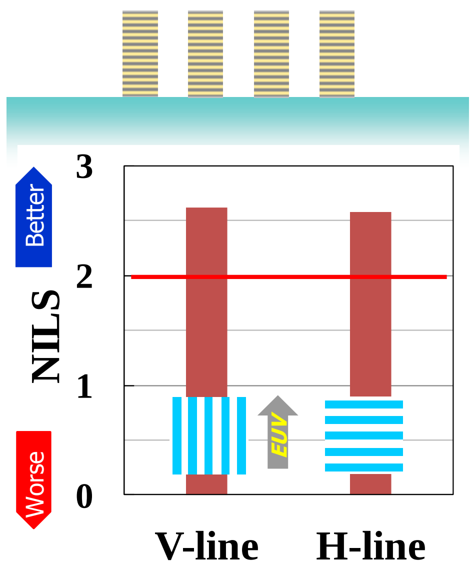
Etched ML pattern has possibility for 4X FF mask.

Ta based absorber

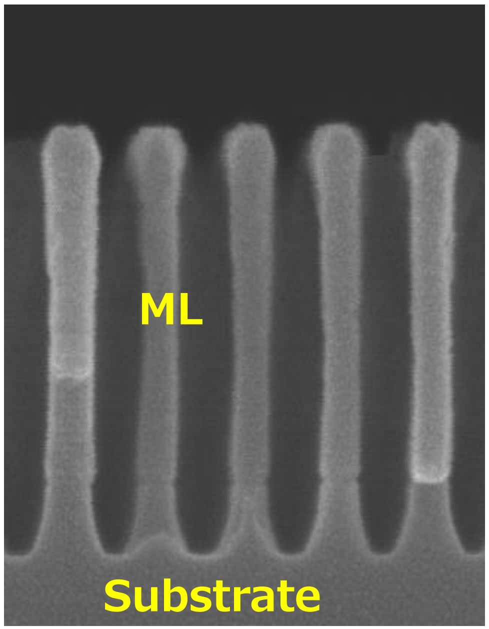


lower mask 3D effect

Etched Multilayer



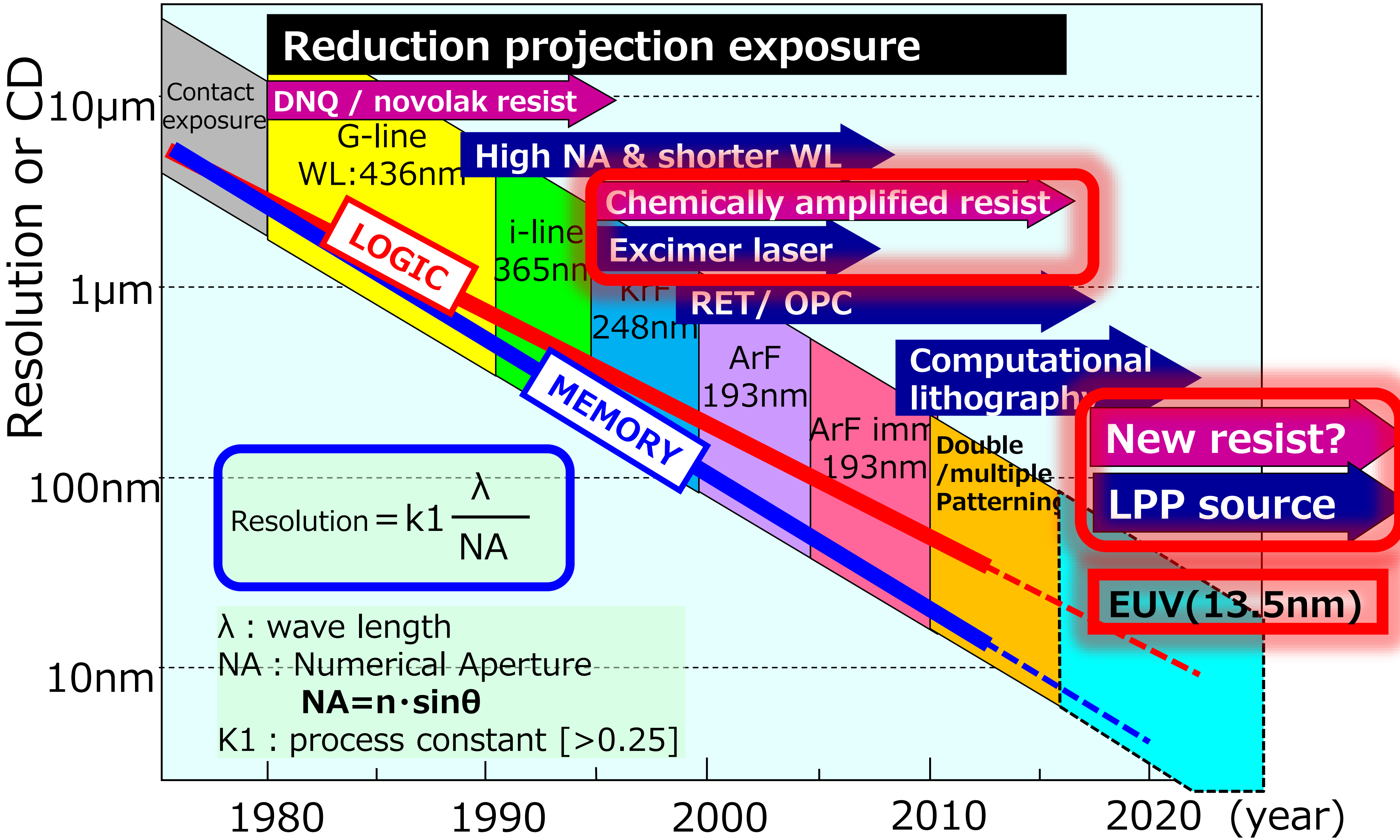
After HM/Ta removal



Takashi Kamo, et al, 2013 International Symposium on Extreme Ultraviolet Lithography

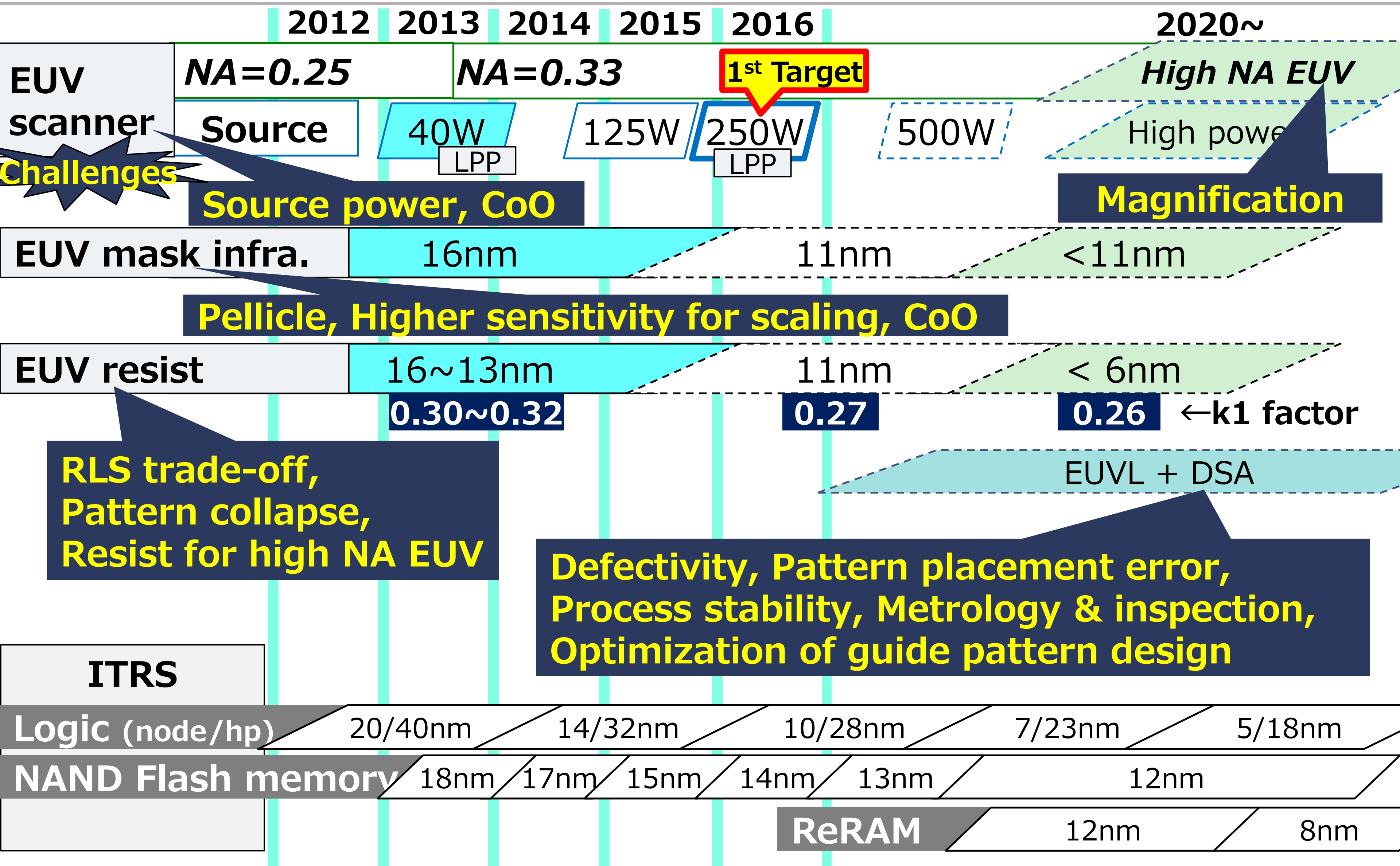
Etched multilayer L/S pattern of 40 nm hp on mask (10 nm hp on wafer using 4X optics) is achieved.
→**Enabler of high NA, 4X full-field and 6 inch mask**

Lithography history



Summary

Trend of EUV lithography



Summary

- **EUVL will to be introduced into logic pilot production in near future.**
  - Source power of > **100 W**
  - Tool availability more than **75 %**

- **More requirements for high volume production**
  - Cost-effectiveness should be considered.
  - **Ultimate high throughput** with > **250 W** source
  - Tool availability more than **95 %**
  - Breakthrough of EUV resist
  - Throughput can be maximized by **high power source** (> 1kW) and **4X full-field 6 inch mask** with etched ML mask for high NA EUV.

Acknowledgment

The author would like to thank ASML

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